EXHIBIT M

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Telephone: (671) 477.9891
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Facsimile: (214) 593-9111

Attorneys For Plaintiffs
Nanya Technology Corp. and
Nanya Technology Corp. U.S.A.

IN THE DISTRICT COURT OF GUAM

NANYA TECHNOLOGY CORP. AND NANYA TECHNOLOGY CORP. U.S.A.,

Plaintiffs,

v.

FUJITSU LIMITED AND FUJITSU MICROELECTRONICS AMERICA, INC.,

Defendants.

Case No. CV-06-00025

DECLARATION OF JOSEPH C. RAZZANO IN SUPPORT OF PLAINTIFFS' SUR-REPLY TO DEFENDANT'S MOTION TO DISMISS

I, JOSEPH C. RAZZANO, hereby declare as follows:

1. My name is Joseph C. Razzano. I am over the age of 21 and am competent to make this Declaration.

2. All of the statements set forth herein are true and correct and are based on my personal knowledge.

3. I am an attorney of record for Plaintiffs, Nanya Technology Corporation and Nanya Technology Corp. U.S.A. ("Nanya" collectively herein), in the above-captioned and titled cause.

4. On June 10, 2007, the Nintendo DS Lite was purchased on Guam at Toys N' Joys which is located in Harmon, Guam.

5. On June 22, 2007, the Nintendo DS Lite purchased in Guam was inspected and confirmed that, in fact, the Nintendo DS Lite contains a device pictured in Exhibit "A" bearing the stylized F mark and bearing Part No. 82DBSO2163C-70L. It is my understanding this mark and Part Number corresponds to a Fujitsu memory device.

6. I personally contacted or directed to be contacted the following locations and confirmed that Nintendo DS Lites are also sold and in some cases have been sold prior to September 13, 2006:

1) Gamestop located at the Agana hopping Center in Hagåtña, Guam.

2) Play N' Trade located at the Guam Premier Outlets in Tamuning, Guam.

3) Uttam's located in Tamuning, Guam.

7. On June 20, 2007, the SonyPlaystation Portables ("PSP") was purchased on Guam at Toys N' Joys which is located in Harmon, Guam.

8. On June 22, 2007, the PSP was inspected and confirmed that, in fact, the PSP contains a device pictured in Exhibit "B" bearing the stylized F mark and bearing Part No. MB44CO12. It is my understanding this mark and Part Number corresponds to a Fujitsu memory device.

9. I personally contacted or directed to be contacted the following locations and confirmed that PSPs are also sold and in some cases have been sold prior to September 13, 2006:

1) Gamestop located at the Agana hopping Center in Hagåtña. Guam.

2) Play N' Trade located at the Guam Premier Outlets in Tamuning, Guam.

3) Uttam's located in Tamuning, Guam.

10. On June 20, 2007, I visited Atkins Kroll and confirmed that Toyota Part No. 83291 corresponds to the Toyota Prius instrument console. I verified with the Parts Department that Part No.

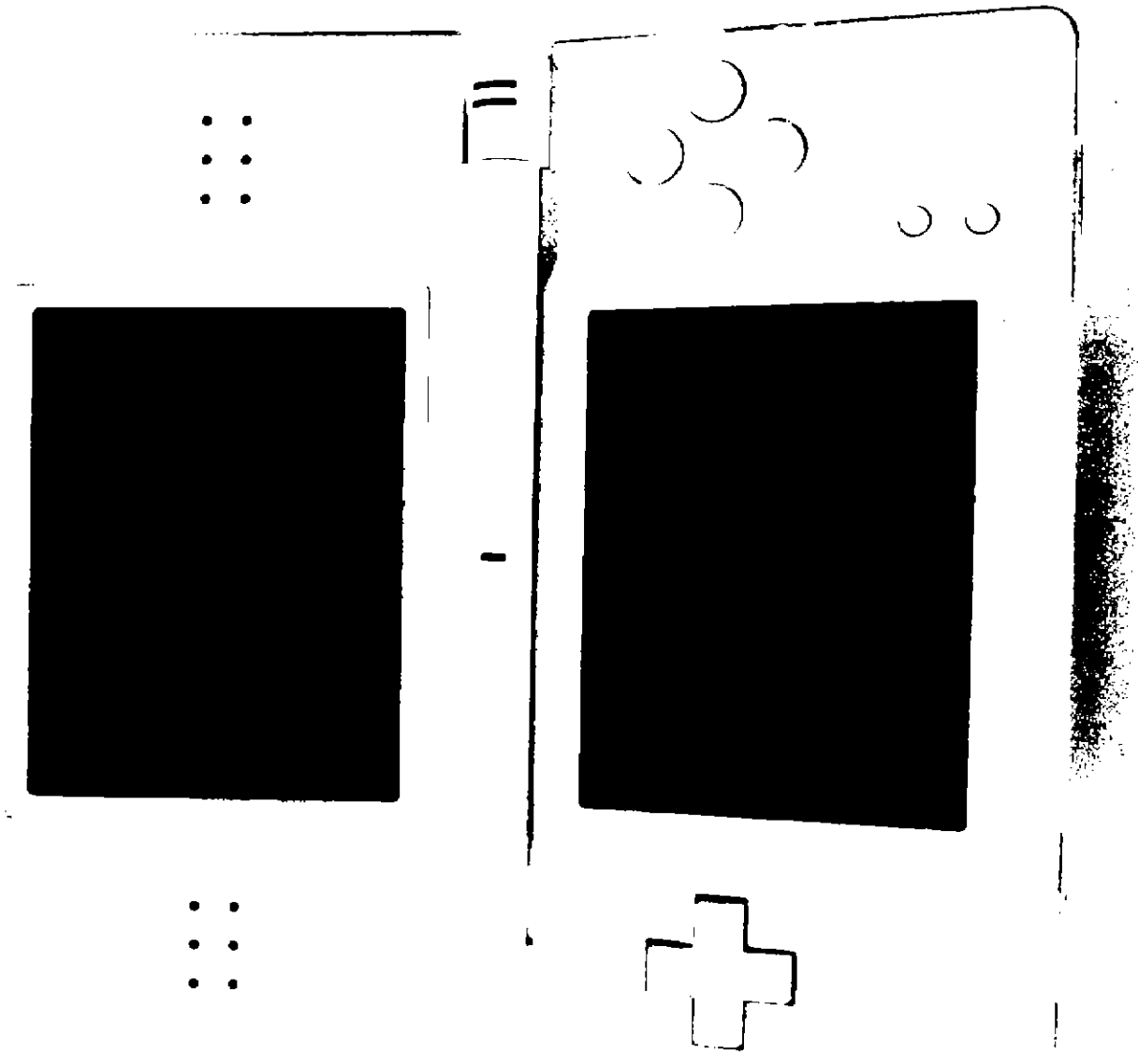
83291 is currently available for sale. The Part Number includes a device bearing Fujitsu Part No. MB90583C and it is my understanding that this is a Fujitsu 16 Bit Micro-Controller, which incorporates Semi-conductor structures that infringe the Nanya Patents-in-suit. See Exhibit "C". I contacted Toyota Sales Department and confirmed that the Prius has been sold on Guam since 1998 in varying quantities between two (2) to four (4) cars per month.

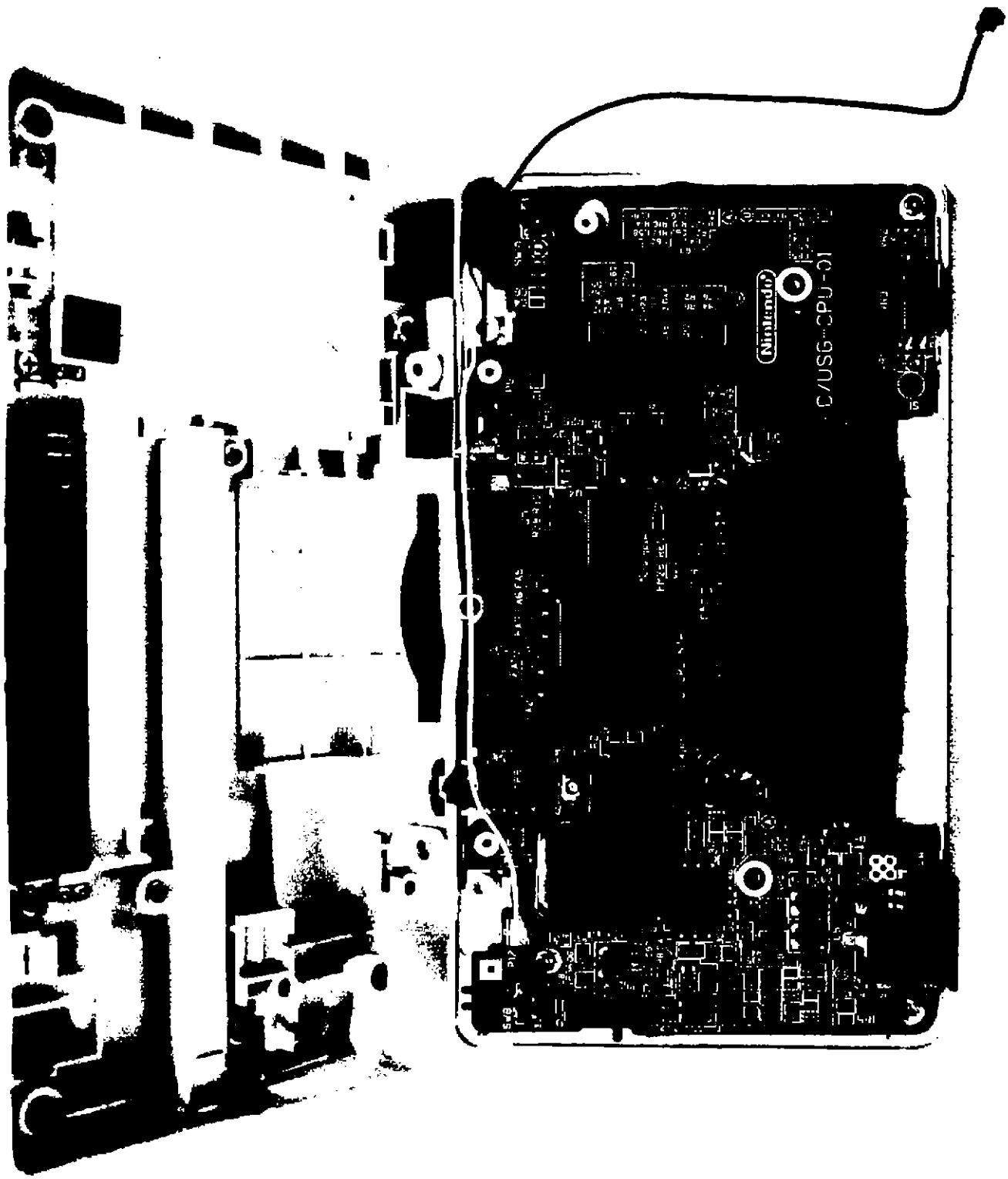
Pursuant to 28 U.S.C. § 1746, I declare under penalty of perjury that the foregoing is true and correct.

EXECUTED on June 22, 2007.

JOSEPH C. RAZZANO

EXHIBIT A

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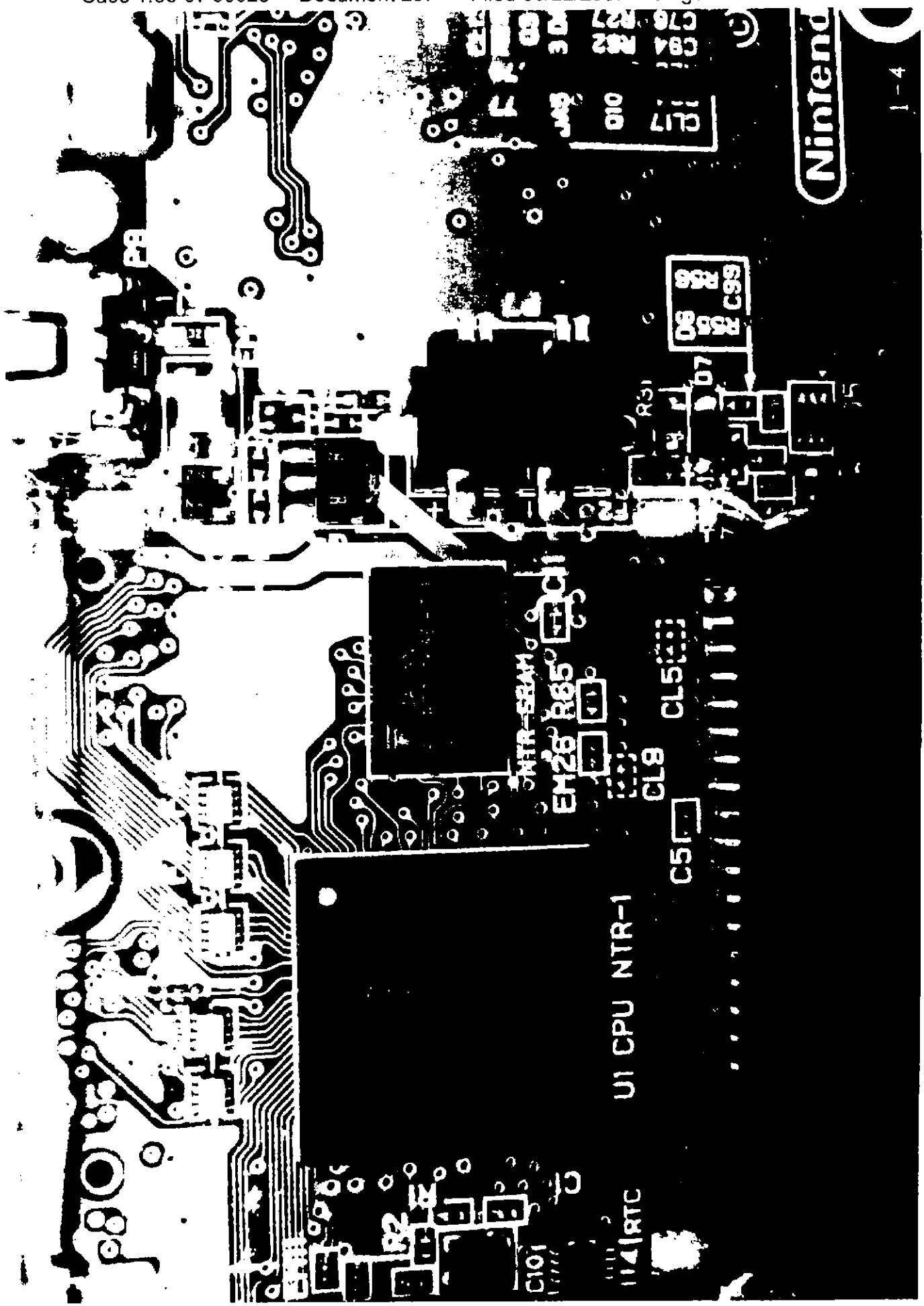
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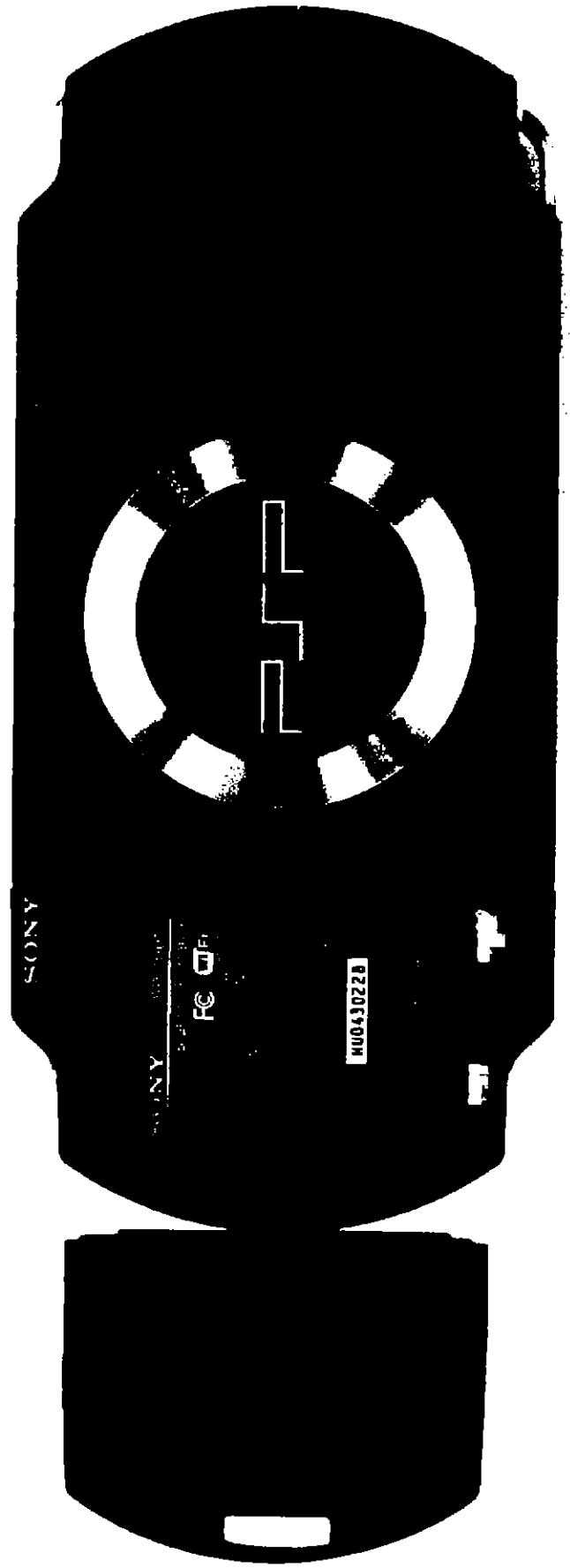
CL8
CL5
C5
RTC

EXHIBIT B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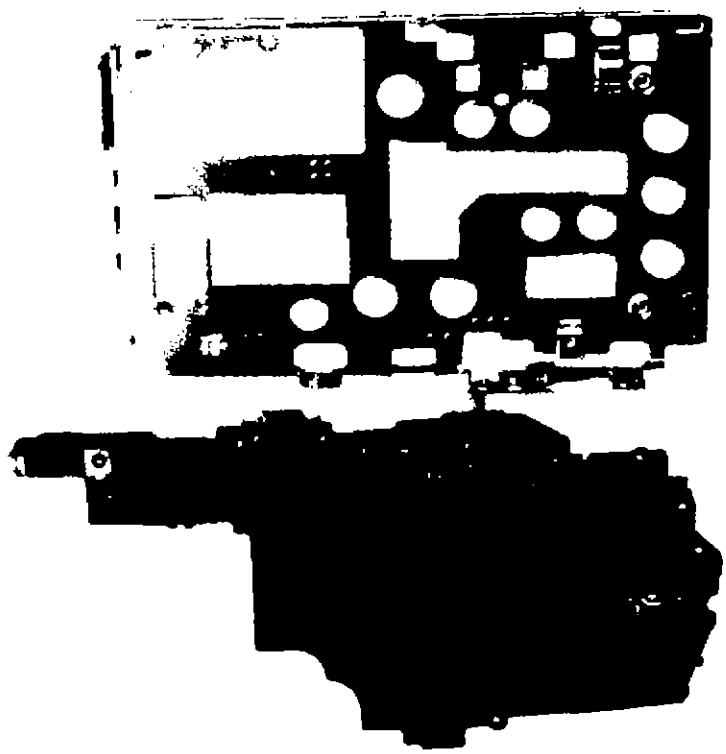
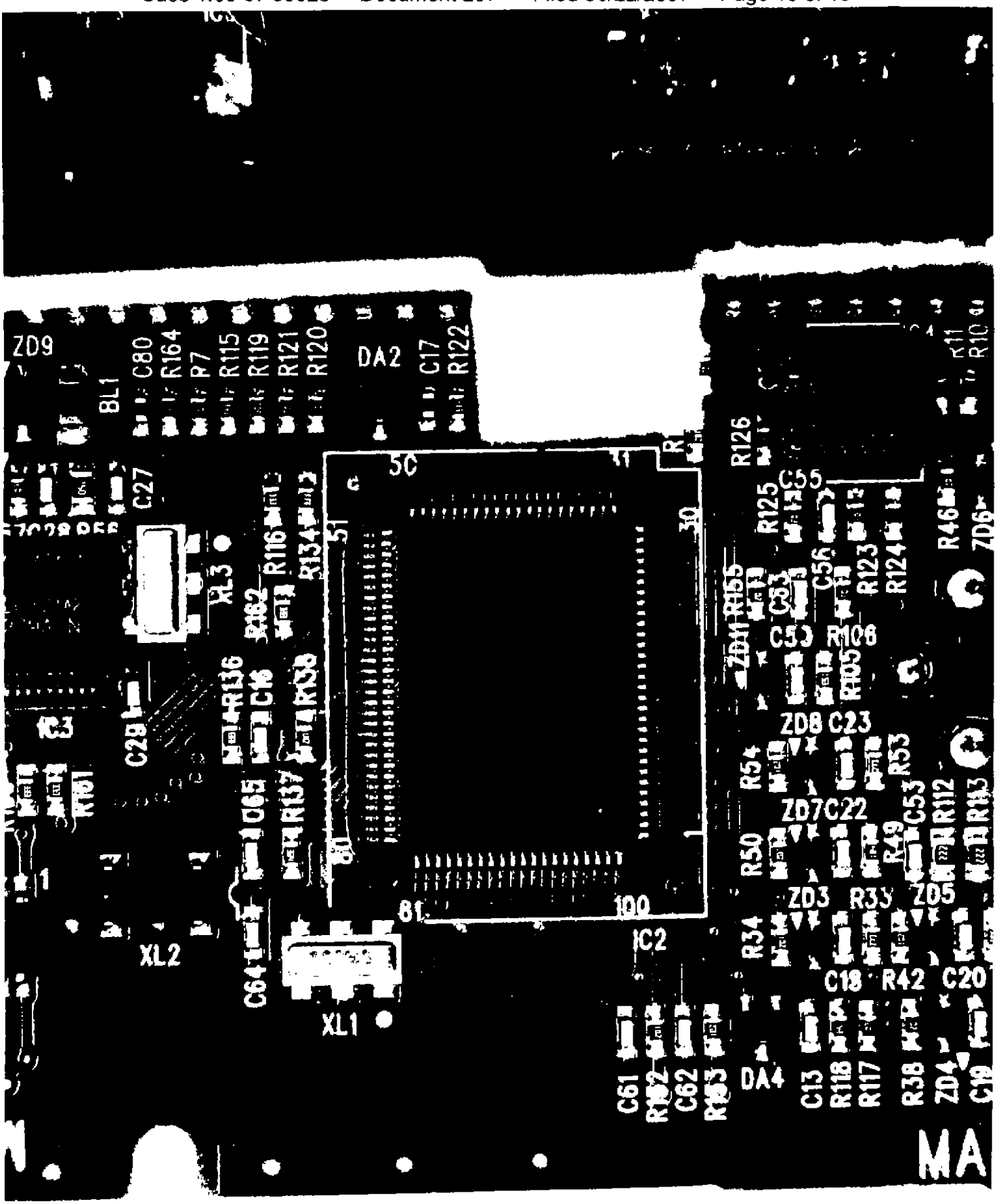
SONY
HU0430228




TA-086
IC7001
>EP GW<
Q003

EXHIBIT C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R164
R7
R115
R119
R121
R120
DA2
C17
R122
C27
XL3
R116
R134
R136
C16
R130
C28
IC3
C65
R137
XL2
C64
XL1
IC2
R126
C55
R125
R46
ZD6
C56
R123
R124
C53
R106
R105
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C23
R54
R53
ZD7
C22
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R49
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R33
ZD5
R34
C18
R42
C20
C61
C62
DA4
C13
R118
R117
R38
ZD4
C19
MA

EXHIBIT N

UNITED STATES DISTRICT COURT
DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A., *Plaintiffs,* v. FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC., *Defendants.*	Case No. CV-06-00025 **DECLARATION OF SANTOS GARZA Ph.D., P.E.**

I, Santos Garza, hereby declare as follows:

1. My name is Santos Garza. I am over the age of 21 and am competent to make this declaration. All of the statements set forth herein are true and correct and are based on my professional practice and personal knowledge.

2. I am a Technical Advisor for Shore Chan Bragalone LLP. I possess a Ph.D. in engineering, am licensed as a Professional Engineer, have twenty (20) years experience in semiconductor technology at Texas Instruments, and teach semiconductor design and manufacturing at the School of Engineering at Southern Methodist University. Additionally, I am registered to practice in patent cases before the U.S. Patent & Trademark Office. As part of my job responsibilities, I research the design, manufacture, and function of semiconductor devices.

3. I personally reviewed the data sheet for Fujitsu part no. MB82DBS02163C-70L, a part I understand is incorporated into the Nintendo DS Lite. The data sheet, titled "MEMORY Mobile FCRAM™ CMOS 32M Bit (2 M word X 16 bit) Mobile Phone Application Specific Memory MB82DBS02163C-70L," describes the Fujitsu MB82DBS02163C-70L device as an

"FCRAM" memory. FCRAM is known in the semiconductor industry as a specific type of Dynamic Random Access Memory or "DRAM," which is the same type of memory the Nanya patents-in-suit are directed toward. My understanding is independently confirmed by the 3 DENALI MEMORY REPORT issue 4 (May 2004), a publication often relied upon by practicioners in the semiconductor industry. A true and correct copy of the DENALI MEMORY REPORT is attached hereto as Exhibit A.

I DECLARE UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE UNITED STATES OF AMERICA THAT THE FOREGOING IS TRUE AND CORRECT.

SIGNED ON THE 25 DAY OF JUNE, 2007

SIGNATURE Santos Garza

PRINTED NAME Santos Garza

EXHIBIT A

May 2004—Volume 3, Issue 4

Denali

Market Analysis and Trends in the Semiconductor Memory Industry

Denali Memory Report

The Denali Memory Report is produced and distributed by Denali Software, Inc. It is delivered free of charge to registrants on Denali's web site, www.eMemory.com. This web site also contains back issues of DMR and other presentation materials from Denali MemCon Conferences, which were launched last year in Boston, Tokyo and San Jose.

In the DMR, readers will find memory market news, discussions of market trends, products and product strategies of memory vendors, alliances and industry technical consortia, and companies' financial performance. In each issue, we have included an interview with an important industry spokesperson, commenting on his company's status or corporate strategy, the outlook for the industry or technical trends within his company's markets.

Denali Software, Inc. is the world's leading provider of EDA tools and Semiconductor Intellectual Property (SIP) solutions for chip interface design, integration, and verification. PureSpec™ is the most robust interface verification solution for key SOC Express interfaces. Denali's Databahn™ product provides designers with the highest quality solution for producing memory controller cores for all of the new and emerging DRAM memory technologies. Denali's MOAV™ product is the de facto industry standard for modeling and simulating memory during all phases of design and verification. Memory selection, memory controller configurations, and memory system performance analysis are supported through Denali's online infrastructure at eMemory.com. More than 100 companies worldwide use Denali's tools, technology, and services to design and verify complex chip interfaces for communication, consumer, and computer products. For more information, please visit Denali at www.denali.com or contact Denali directly at: (650) 461-7200, or email info@denali.com.

In This Issue:

MEMORY INDUSTRY UPDATE

INTERVIEW

Register now for Denali's User Group at DAC!

www.denali.com/dac2004.html

Monday, June 7, 2004 • 5:00pm-9:00pm
San Diego Convention Center • DAC Rooms 31ABC, 32AB

Denali Software, Inc.
info@denali.com • www.denali.com • www.eMemory.com

Analyst: Lane Mason • Managing Editor: Jonah McLeod • Production Designer: Alissa Wyffels
Publisher: Kevin Silver

Denali

MEMORY INDUSTRY UPDATE

Memory Industry Outlook

Business continues to strengthen, but, as well, a positive outlook does have its detractors. This suspicion, backed up by anecdotal data and a factual history of failed 'upturns' in the past several years, has continued to keep a lid on spending, expansion of supply, and the 'go for the gusto' attitude of wild spending and investment that eventually prevails, and, in so doing, plants the seeds of every upturn's eventual demise.

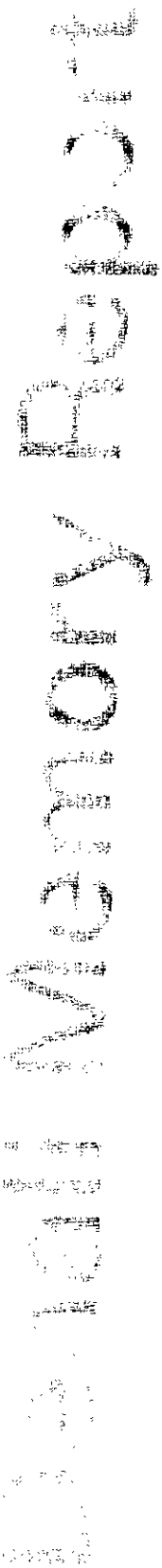
The financial results for memory vendors in 1Q04, shown in the article below, were much, much better that 4Q03. Only a few laggards are still running red, and most companies were firmly in the black, after three years of losses, downsizing, and suffering. Midway through 2Q04, the outlook continues to be positive for memory vendor profits.

The mixed signals are coming from the PC market, where various analysts are saying the market (1) will grow, (2) will be flat, or (3) will shrink in 2Q04. For sure, some overbuying in 4Q03 left inventories higher than hoped for or needed, and scavenged some sales from early in 2004 back into 2003. Intel's new DDR2-supporting Grantsdale chipset is nowhere to be seen. Laptops and desktops continue to sell into a price-pressured environment where price, and not new features, is the driving force. But, 'consumer digital' is all the rage today, and is starting to drive a lot of silicon demand. Cell phones continue to be a strong market, and are today, about 40 percent as large a silicon market as computing, and devouring an increasing share of the industry's output. The superficial picture is hardly clear, but we continue to believe that the overall business is strengthening, and will continue to do so, against an increasingly tight chip supply. One can even argue, that, like the US economy, we are already more than two years into a recovery, but were so deeply mired in economic weakness, that it takes a long time to grow enough to break through the surface and set new highs.

The most telling indicator, we feel, is leading edge foundry capacity. UMC and TSMC tell us that they are both running 100 percent of capacity or more. DRAM prices were up more than 20 percent in the past two months, refilling inventories and adapting to the shift of large amounts of capacity to flash, PSRAM/SRAM, foundry and logic. Eternally optimistic that the profit upturn was just around the corner for most of three years, DRAM makers were slow to reallocate substantial amounts of their capacity away from the massive DRAM losses they were suffering. But starting mid-2003, they DID have alternatives to shipping a $2 bill with each DRAM. They started more PSRAM wafers for cell phones, CMOS image sensors for cell phones and other applications, and started taking in foundry for flash and logic. For those lucky enough to have an established position in NAND flash, they tried to quench the insatiable thirst for bulk bits in dozens of consumer-media applications. Things have moved slowly, given the severity of the downturn, but the wheels have started to move, stabilizing prices and improving profitability.

Table 1. is our forecast (extending the WSTS database) for the coming year: five quarters 'actual' data from the SIA, and three quarters forecast from Denali:

	1Q04	2Q04	3Q04	4Q04	1Q04	2Q04E	3Q04E	4Q04E	Yr 2004
DRAM	3482	3472	4623	5112	5450	5850	6300	7500	24800
SRAM	652	628	650	702	712	788	826	886	3232
Flash	2278	2415	3072	3973	3880	4200	4730	5090	17880
NOR					2274	2300	2480	2600	9584
NAND					1606	1900	2250	2490	8296
Other	339	346	374	413	382	380	410	420	1582
Total	6751	6842	8705	10209	10464	11030	12260	13820	47974
	40.1%	1.3%	27.2%	17.3%	2.5%	5.4%	11.2%	12.7%	



Denali Corner

Denali MemCon Boston is a Great Success
On 13 May, Denali hosted its third Denali MemCon Boston at the Westford Regency in Westford, MA. This one-day event featured speakers from a dozen semiconductor industry companies. For the entire conference program and presentation see **www.eMemory.com** (click "research").

The conference began with a keynote from Dr. Randall Isaac, Vice President of Strategic Alliances at IBM Technology Group. His witty and insightful talk described the quest for the universal memory and examined the potential for every conceivable memory technology including rotating disk drives: DRAM, SRAM, flash, and the numerous alternative memories vying to replace these commodity parts: MRAM, etc.

A talk by Larry French, Micron Technology's Computing and Consumer Group FAE Manager, detailed the evolution of DRAM memory for the latest computer designs, describing the performance advantages and enhancement offered by DDR2 versus DDR1 DRAMs. He also touched on the company's RLDRAM offering and concluded with a discussion of DIMM packaging.

Another highlight of the conference was a presentation by Pete Vogt, Principal Engineer at Intel, who described the industry's rationale and roadmap for the fully buffered DIMM (FB DIMM). The roadmap starts as a high-speed solution in servers with the FB DIMM populated with DDR1 memory components and migrates to the higher speed DDR2 and later devices over the rest of the decade.

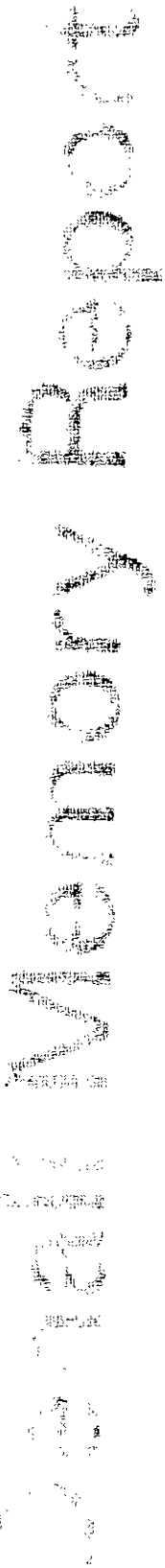
For ASIC designers struggling with integrating their chips with the latest high-speed memory, Michael Ching, Product Marketing Manager at Rambus and Masood Ghamaty in technical marketing at Artisan both detailed interface solutions for DDR2 memory in their individual presentations. Concurrent with the conference, Rambus announced plans with Denali to jointly provide DDR memory system solutions (see the release below) and demonstrated their DDR interface running at 1.6GHz at their booth.

Lalitha Oruganti, Product Marketing Engineer at Altera described her company's Stratix II FPGA's ability to drive a DDR2 interface at 533Mb/s. At the Altera booth, she even had two demo boards populated with Stratix EP1S40 FPGA with Le Croy scopes connected that showed high-speed data transfers for DDR1, DDR2, and RLDRAM, running at 400Mb/s data rate.

Shigeo Ohshima, Senior Manager, SoC Research and Development Center at Toshiba described his company's roadmap for FCRAM and provided insight into the latest member of the family, FCRAMII+, for which a spec has now been finalized, as well as the newly emerging Rambus-initiated XDR high speed memory architecture. Michael Pearson, Director of Network Business at Samsung Semiconductor Inc. detailed the QDR consortium's latest offering the QDRIII—for the network equipment designers looking for the highest speed SRAMs available.

Eugene Chang, Senior Marketing Manager at Infineon carried the torch for flash memory. His presentation provided a survey of NOR, NAND and Infineon's new Twin Flash offering, which plays in both NOR and NAND spaces. The presentation was complete with market data and competitive advantages and disadvantages for the various flash memory types.

Bill Wang of VeriSilicon presented an insightful view of the emerging China foundry market, labeling the players, defining the different ways business is done in Mainland China, and providing a view into the explosive market potential for consumer electronics in this emerging economic power. His charts on monthly wafer starts for the major China fabs were very informative, given the right capacity fabs worldwide are facing.



The Denali team also did their part for the audience. Memory Market Analyst Lane Mason provided a memory market update, and pointed to consumer and flash memory as drivers for memory growth this year. Still, he noted that PCs consume the lion's share of the DRAM market and account for about 90-95 percent of megabyte shipments.

Product Marketing Manager Vic Juneja described Denali's unique verification IP solution Memory Maker Advanced Verification (MMAV) and how it models every class of memory made today, with all these models—several thousand in all—available online at Denali's **www.eMemory.com** web site. Mike McKeon, Director of Strategic Products detailed Denali's Databahn product, a highly configurable, silicon-proven memory controller that can drive DDR2 memory at the high data rates today's memory systems demand. McKeon also cited Databahn's ability to reconfigure quickly to meet designers' changing design requirements from inception to silicon.

Denali News Releases, April and May '04

VeriSilicon and Denali Team to Deliver DDR Memory Interface Solutions for China-based Wafer Foundries (May 13, 2004) VeriSilicon Holdings Co., Ltd., the leading intellectual property (IP) and design service provider for China-based wafer foundries, and Denali Software today announced a partnership to provide silicon-proven memory interface solutions for those foundries. This announcement is being made during Denali MemCon, the yearly forum for exchanging information about semiconductor memory and PCI Express technology, hosted by Denali, provider of electronic design automation (EDA) solutions for chip interface design and verification. (See the entire release at **www.denali.com/news_pr20040513b.html**)

Rambus and Denali to Provide Complete DDR Memory Controller Design Solutions; Enables Integration of Physical and Logic Layers, Reducing Risk and Improving Time to Market for Memory System Makers (May 13, 2004) Rambus and Denali announced plans to jointly provide DDR memory system solutions. Combining Rambus drop-in DDR interface cells with Denali's Databahn DDR controller IP provides chip designers with an integrated design environment that will reduce risk and improve time to market when developing and verifying DDR memory controller interfaces. (See entire press release at **www.denali.com/news_pr20040513a.html**)

Denali Launches PureSuite, First Comprehensive Verification Suite for Compliance, Interoperability of PCI Express Designs; Automated Solution Reduces Time, Risk Associates With Functional Verification (May 10, 2004) Denali introduced PureSuite™, a comprehensive verification suite that exercises PCI Express designs and measures both compliance with the PCI Express specification and interoperability with other PCI Express designs. PureSuite, together with Denali's popular PureSpec™ verification IP product, provides a completely automated solution for functional verification of PCI Express designs. The PureSuite product enables designers to dramatically reduce the time and risk associated with functional verification, a task which regularly consumes over 70 percent of the entire chip development cycle. (See entire press release at **www.denali.com/news_pr20040510.html**)

Denali Sublicenses Databahn DDR Controller IP Cores to IBM; IBM ASIC Customers to Access DDR1/DDR2 Controllers for 90nm and 130nm Copper (April 19, 2004) Denali announced it has signed an agreement enabling IBM to sublicense Denali's Databahn™ IP to its ASIC customers, and for internal use on its own chip development efforts.

The agreement covers Databahn memory controller cores for DDR1 and DDR2

technology on IBM's 90 nm Cu-08 and 130 nm Cu-11 processes. The flexibility of the Databahn memory controller to support multiple configurations and memory architectures is accomplished through a synthesizable core. Support of high-performance applications is possible by hardening critical timing circuits such as Denali's proprietary Delay Compensation Circuitry (DCC). (See entire press release at **www.denali.com/news_pr20040419.html**)

Denali at the 2004 Design Automation Conference

Denali Software will have a major presence at the 41st Design Automation Conference to be held at the San Diego Convention Center June 7 through 11. For more information on the conference click **www.denali.com/dac2004.html**. If you plan to attend please check out the activities listed below that Denali has planned.

- **Denali DAC Booth/Demo Suite #1945:**
  Schedule a meeting: **info@denali.com**
- **Denali Users Group Meeting:**
  Monday June 7, 3-9PM DAC Rooms 31ABC, 32AB
  Register to attend: **www.denali.com/dug/**
- **Denali DAC Party:**
  Tuesday June 8, 8PM, On Broadway, 615 Broadway
  Tickets: **www.denali.com/dacparty.html**

Network Memory Update

MemCon Boston provided us with the opportunity to update the market status of both the low latency DRAM, RLDRAM and FC Network RAM, and QDR SRAM. The market for both families of DRAM and SRAM have changed quite a lot with the steady retreat of the networking space as a business opportunity, but appears to have stabilized today as regards committed suppliers to both the DRAM and SRAM camps. The roadmaps leading to higher densities and higher performance devices have also been clarified and extended.

Low Latency DRAMs

In the low latency DRAM (LLDRAM) marketplace, today the market is divided between the FC Network DRAM and the Reduced Latency (RL) DRAM. The FC Network DRAM (FCRAM) is supported by Toshiba and Samsung; the RLDRAM (First generation, RLI), is supported by Infineon and Micron; the RLII is supported only by Micron. FCRAM pioneer, Fujitsu, does not participates in the high density FCRAM market that are used in networking, but only has lower density FCRAMs used in cell phones for their low power attributes.

Both Samsung and Toshiba are shipping 288M FC Network DRAMs, while Toshiba announced its 576M FC Network DRAM in April 2004. Toshiba also announced its enhanced second generation FC Network RAM, FCII+, at this month's MemCon.

In our conversations with Denali customers, it has usually, but not universally, been the case that those companies looking at low latency parts like the RLDRAM datasheet better because of what they feel as its superior feature set and power. In addition, the comment is often made that the RL was designed specifically for the networking applications, while the FCRAM design was driven by a broader and fuzzier applications concept.

However, the relative turbulence in the RL roll-out, setting of the specs and hitting the spec with real-life silicon, has been problematic. RLI was announced in 4/01, but there was no silicon until late in the year, and even that which could be had had a hard time meeting the speed spec. No sooner than RLI started shipping than RLII was defined and announced, along with Micron as a second source to RLDRAM originator Infineon. This roll-out also took time, and Infineon's late 2003 withdrawal from the RLII camp was no help, either. Declining market opportunities in the networking space made it tough to close anyone's business plan.

While perhaps not as 'glamorous' as RLDRAM, FCRAM was in fact earlier to the market, relied on Fujitsu and Toshiba as dual sources. Toshiba and Fujitsu got many early design wins, with real silicon in the more modest performance range—both on overall clock speed and tRC—against Infineon's difficulty in hitting its timing and silicon delivery targets. Having Samsung join in added a credible supplier with good technology in place of Fujitsu, which was always considered a 'marginal' FCRAM and DRAM supplier.

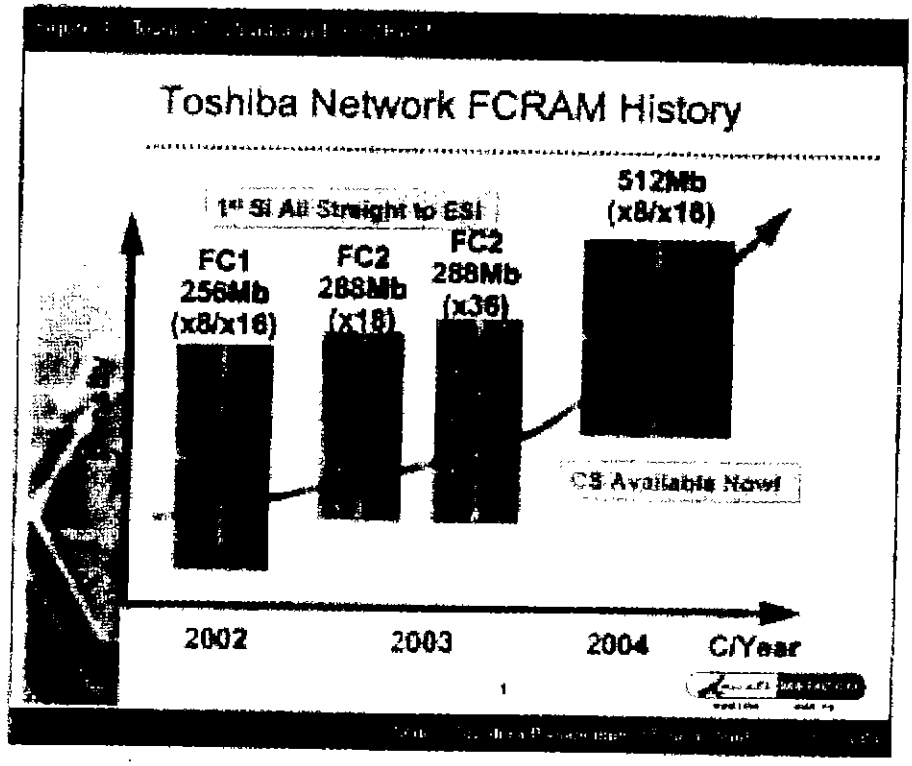
Today, as shown in Figure 1 below, Toshiba has ambitious plans for furthering the FC Network RAM roadmap. They announced a 576M FC Network RAM in April, and clarified their FCII+ technical spec (rumored for many months) at the same time. 576M FC Network RAM II+ are scheduled for delivery mid-2005, with production for later in the year. Toshiba and Samsung work closely together on the FC Network RAM specs to ensure compatibility.

Toshiba's newly announced FCRAMII+ (Figure 2) offers high speed (400MHz clock), burst length of 2, 4 or 8, a single die for x9, x18 and x36 (which was another first generation LLDRAM issue for both FCRAM and RLDRAM, as initial offerings were both with and without parity bits and did not cover all widths that the market needed).

On the RLDRAM side, Micron has worked very hard against the added burden of now being the only supporter of the RLII roadmap. But, Micron has cultivated applications for RLDRAMs outside the networking space, in such places as high-speed L3 caches, to enlarge the RL market and counter the shrinking LL DRAM market for networking alone.

Of special interest in the RL roadmap, as shown in Figure 3, are a few things.

First, Micron has plans to push the performance up to the >667MHz clock range by 2006. Today, Micron is offering 400MHz RLDRAMs, which are as fast as the FC Network DRAM roadmap shown today. Although Micron (and its RL customers) are sensitive to the absence of an RLII second source, Micron continues to try to get this relationship in place, from among other DRAM suppliers and even those with



576Mb Future FC2+ spec ~ now finalized ~

- Number of banks : 8 bank
- I/O Organization : x9, x18, x36 with one chip solution
- Clock Freq & tRC : 400MHz+(800+Mbps) & tRC=<20ns
- Function :
  - Read/CAS Latency(CL) : 5,6 and 7(8)
  - Write/CAS Latency(WL) : CL-1
  - Burst Length : 2,4 and 8
  - Data Strobe : Uni-directional Differential DS,QS
  - New Features
    1) ZQ Type OCD, 2) ODT, 3) QVLD
    4) Multi Bank Write, 5) External Bank Refresh
- Power Supply Voltage: 1.8V(1.5V capability considered)
- Interface(VddQ): SSTL-1.8 & HSTL (1.8~1.5V)
- Package : 144 ball mBGA, 0.8 x 1.0mm ball pitch with JTAG
- Schedule: ES in 2Q'05, CS in 3Q'06, VP in 4Q'06

2

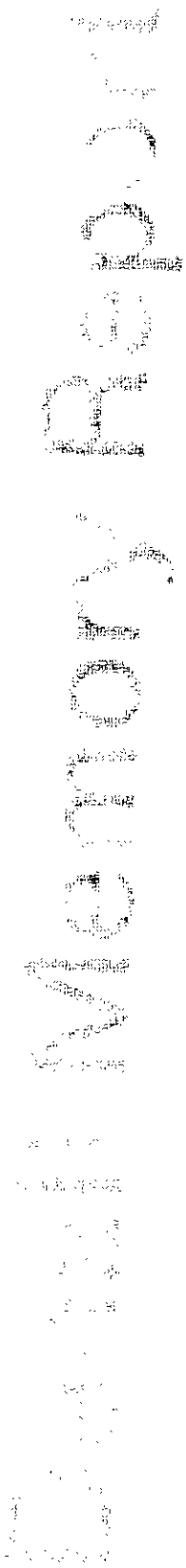
a different stake in the networking space, but not DRAM makers. They claim no loss of design win and interest in RLDRAM due to this lack of an alternate source for RLII.

They also highlight the features of RL (compared to their reading of the FCRAM spec) in that RLDRAM has lower power, already offers a 1.5V operation option (vs. FCRAM's

RLDRAM Advantages

- ❑ Fast tRC (15ns–20ns)
- ❑ 2, 4, and 8-word burst
- ❑ Low bus turnaround
- ❑ Separate I/O for 100% utilization - balanced R:W data flow
- ❑ 1.5V or 1.8V I/O
- ❑ On-die termination
- ❑ Growing infrastructure
  - Reference designs
  - Denali, HSpice, IBIS, Verilog, VHDL, BSDL
  - Much more...
- ❑ 400MHz clock now!
- ❑ Lowest system cost
- ❑ Lowest system power: <½ of competition
- ❑ Lowest signal count in multiplexed mode
- ❑ 400MHz, 533MHz, 750MHz and up to 1.1Gb in 2006

3



'under consideration'). RL's separate I/O advantage. Despite Micron's pull back from SRAMs, and especially the networking SRAM market—ZBT, QDR SRAMs, which they sold to Cypress last year, Micron seems committed to investing and developing the RLDRAM market as a part of its non-commodity DRAM business thrust.

Micron and Infineon maintain a current RLDRAM website, **www.rldram.com**, which gives up-to-date presentations, technical articles and discussions, and development activities.

The low latency DRAM market has also been hindered by other changes and misconceptions that have been clarified over time, in addition to the more limited networking market opportunity faced by the networking majors for their own systems.

The low latency DRAM market was viewed and discussed as a 'derivative of the standard DRAM', implying that it could feed off the technical developments of the high-volume standard DRAM roadmap. In fact it could not. It led the PC DRAM roadmap by perhaps as much as two years in performance, and broke new ground ahead of the volume PC DRAM—sometimes painfully. It moved to leading edge process geometries sooner. It had to deal with power problems sooner. And it needed to deal with high clock rates faster than the PC DRAM and more nearly as fast as graphics DRAMs (but at higher densities, since GDDR only in the past year has offered 256M GDDRs, while RL and FC started right off with 200MHz+ clock speeds—or faster for RLI, which targeted 300MHz in its early datasheets).

The next issue, which has changed the marketplace for low latency DRAMs, is the fact that DDR1 and DDR2—standard PC DRAMs, have emerged as very high performance parts. One can get DDR1 DRAMs up to DDR 550—a 275MHz raw clock speed. But more importantly, DDR2, for which DDR2-667 DIMMs can be had on the market today, had the other advantages of DDR2 over DDR1: power, on die termination, and other features.

So, since some of the early low latency DRAM applications truly were only looking at the raw bandwidth, which they thought they could only get with a niche LLDRAM, and not the low latency per se, they now had an widely sourced DDR2 part, which offered all the high bandwidth benefits and none of the higher-pricing, and cluttery roadmap and uncertainties of the LL products. Besides, DDR2 did offer some improvement in 'natural latency', from about 55ns for DDR1, down to 45ns—nothing like the <20ns tRCs for true LLDRAMs, but sometimes good enough for certain applications.

QDR SRAM Roadmaps

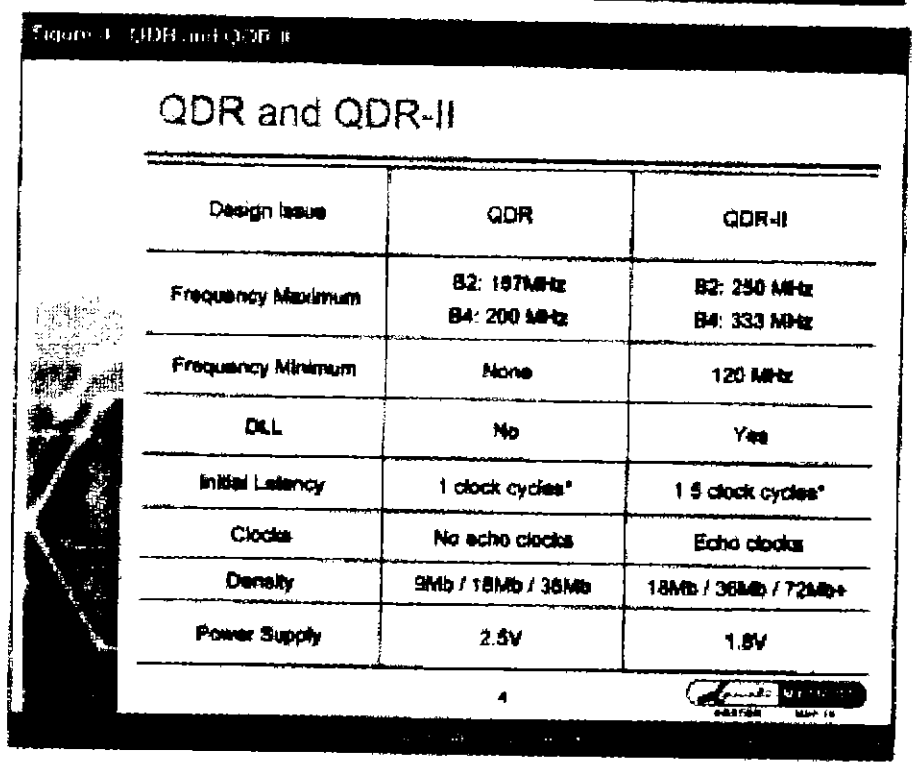
Since a year ago, many marginal QDR suppliers have pulled back on their efforts, and SigmaRAM proponents have either capitulated to the momentum of QDR, or withdrawn entirely. Overall, the network SRAM market supplier base is down by half since 18-24 months ago, but seems rather stable today: Cypress, Samsung, IDT, Renesas and NEC.

On the SRAM side, the QDR camp is now shored up as the earlier competition from SigmaRAM has faded. At Denali MemCon Boston, Samsung's Mike Pearson presented an update on QDR II and QDR III products, in which he spoke for not only Samsung but also the QDR consortium as a whole.

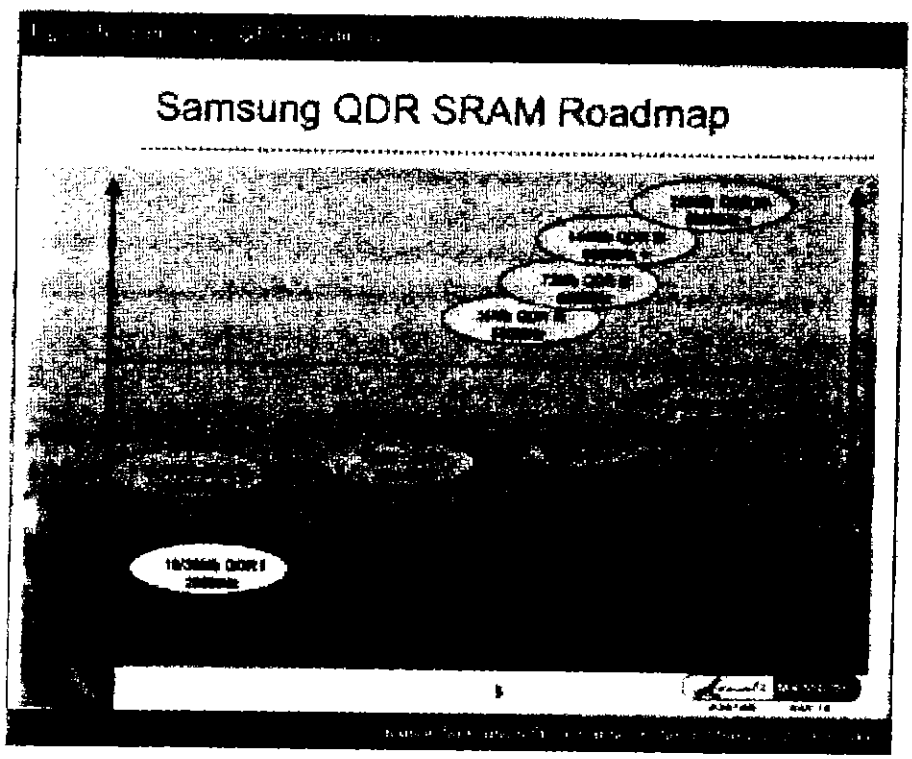
Like the RLDRAM, the QDR Consortium maintains a current website at **www.qdrsram.com** which keeps users updated on the status of the market.

QDR II is today the mainstay QDR SRAM family being used, and is shown in comparison with QDRI in Figure 4 on page 9. These offer densities up to 36M and clock rates up to 250MHz, available from most of the QDR consortium members.

Samsung's QDR roadmap shown in Figure 5 on page 9, extends their effort into the next generation QDR, QDR III, which is now being fully defined by the consortium: More density, higher clock rates.



It should be noted here that most QDR suppliers also have companion DDR2 SRAMs of comparable of faster speeds, which are widely used in the networking marketplace—same high speeds as QDR, but no separate I/Os operating to independent clocks, as in QDRs. Samsung is probably the leader here in DDR2 SRAMs with 300-500MHz clocking.



taking over the HS SRAM market from IBM, which held a resounding lead from 1996-2001 when HS SRAMs were driven mostly by the workstation and server caches market.

Networking RAMs Future

Both the QDR and LLDRAM marketplaces serve applications requirements that are unreachable with any assembly of standard DRAMs or SRAMs, and are therefore, 'permanent niches' not likely to be washed out by whatever good or bad economics that niche RAMs often face. One can achieve the LLDRAM functionality with many Standard SRAMs, but only at a cost perhaps 10x that of the RL or FC Network RAM; the dual-portion of QDR SRAMs is pretty much out of reach for any standard components assemblage. The future rests with vendors designing to the network customer's changing roadmaps, perhaps adding some special functionality as a superset of the consortium's QDR standard, or being first to the next highest speed bin.

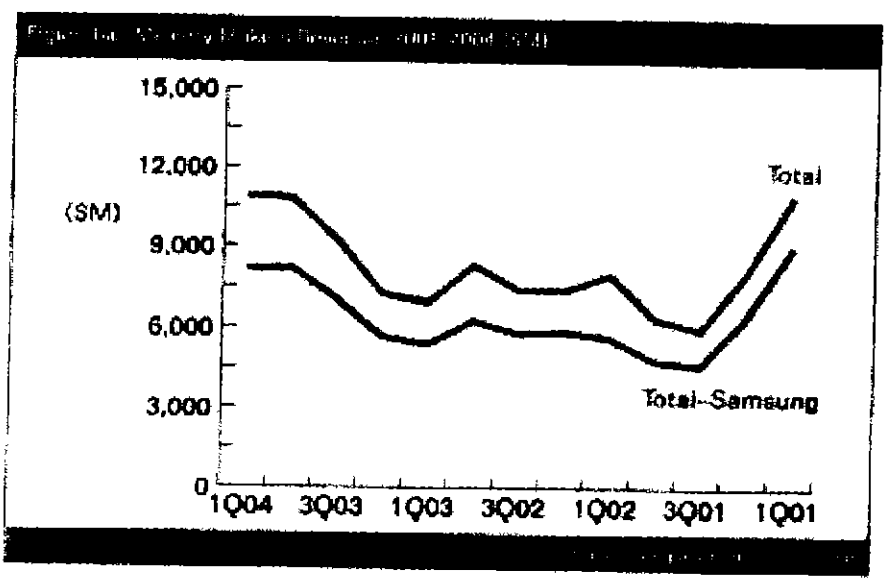
As we've discussed in earlier DMR interviews, these networking parts have terribly long design-to-production lifetimes, which make it necessary for both vendor and user to set their marketing plans, their product development budgets and expectations accordingly. These are not commodities. It takes longer to recover the initial investments (for vendors) and the product lifetimes are far longer than traditional SRAMs and PC DRAMs. As such, they are actually network ASIC memories, customized for a small group of users. Perhaps, then, as they have been rumored from time to time, these parts might be candidates for user-defined and user specified custom "system specific memories," with all the proprietary features, restricted distribution and high-value-add system performance implied by that action. (The topic of 'custom memories' and 'user-defined' chips will be the topic of discussion in the next DMR.)

Company Financials for 1Q04

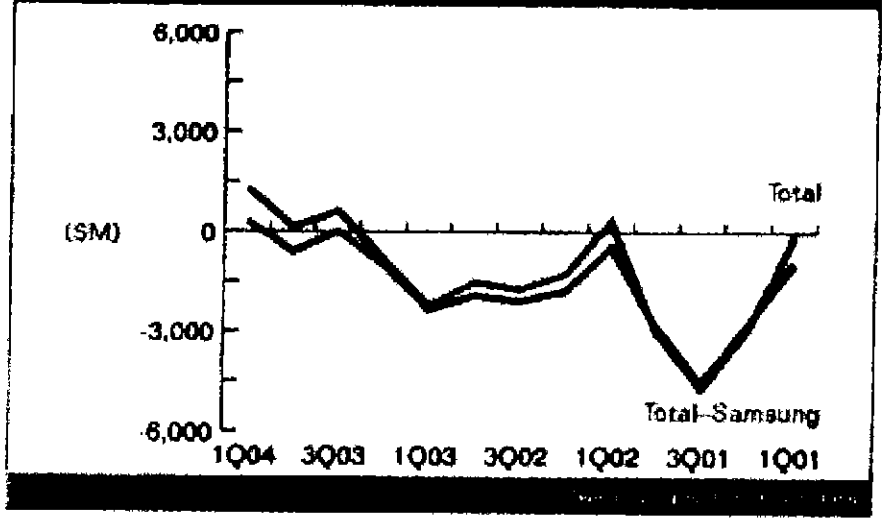
Most companies reported their 1Q04 results within the past 10 days, and those results are compiled in Table 2, below. Everyone except Micron, whose fiscal quarter leads the industry by one month, showed improved results from the prior quarter; some, markedly so.

This time, the table shows the company detail with some summary data at the bottom: industry totals with and without Samsung, which recently has constituted 25 percent of memory industry sales and (net) all of its profits.

The profit trend lines are even more telling. Figure 6a shows the revenue for our set of memory makers since 1Q03, and Figure 6b shows the profit (again, with and without



Company	1Q04 Sales	4Q03 Sales	Change	1Q04 Profits	4Q03 Profits	Change
AMD Flash (Spansion)	628	566	11.0%	14	3	NM
Atmel	407	380	7.1%	11	11	0.0%
Cypress	254	238	7.0%	27	23	17.4%
[illegible]	[illegible]	[illegible]	9.1%	7.7	2.3	234.8%
Infineon	797	812	-1.8%	16	72	-78.3%
ISSI	520	40	30.0%	13	0.9	1288.9%
Sandisk	387	388	-0.5%	64	88	-27.3%
ST Micro	462	459	1.3%	5	1	400.0%
SST	104	95	9.2%	14	9.1	56.0%
[illegible]	116	97	19.6%	34	10.8	214.8%
Winbond	247	239	3.3%	20.6	6.1	236.1%
[illegible]	[illegible]	[illegible]	[illegible]	0.6	-33	NM
Micron	991	1107	-10.5%	-39	1	NM
[illegible]	[illegible]	[illegible]	[illegible]	31	18	72.8%
Powerchip	326	247	32.0%	100	48.9	104.5%
[illegible]	[illegible]	[illegible]	[illegible]	NA	NA	NA
Ramtron	32.5	32	0.3%	8.3	8.6	-3.5%
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	279	22.9%
[illegible]	[illegible]	[illegible]	4.6%	965	741	32.9%
Hynix	1226	1012	21.1%	303	-889	NM
Intel/Other	[illegible]	[illegible]	0.4%	-319	-97	NM
Subtotal	5015	4678	7.3%	1069	-245	NM
Sum	15145	14454	4.8%	1963	401	389%



Samsung) since 1Q03. In case of the profits, we have taken the liberty of estimating comparable after-tax profits for those companies for which we only had pretax or operating profits (those for which memories are a single product line in a larger company: AMD/Spansion, Samsung, ST Micro, etc.).

Most of the outlooks given in the analyst calls for 1Q were positive for 2Q04, and for the year, but were couched with hesitation that 'the picture was not entirely clear, and the future was unknowable.' We're all reading from the same tea leaves.

As with late 2003, it should be noted that Samsung, using any reasonable measure of the tax rate to be applied to its chip operating profits, had a disproportionate share of the total industry's profits. Indeed, to update a table that we published six months ago, comparing Intel and Samsung's financial results (then, 3Q03, this time 1Q04), we find again that Samsung Electronics (which includes profitable display business and their leadership high-end cell phones) is comparable to Intel, who has ridden the MPU/PC market for more than a decade:

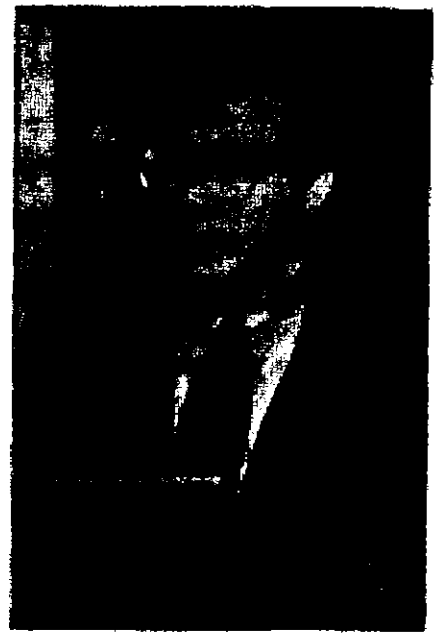
One could argue that Intel could look much better if it would jettison its non-MPU businesses, but one has to be impressed that Samsung can look about as good as Intel, even as all their memory competitors are sloshing about in a bath of mostly red ink. This is not monopoly profit, holding the competition at bay with patents, or marketing strength. It is low cost production, a product portfolio that spans enough markets that there is always some that are higher margin than others, and considerable production agility to shift production, and give up market share in losing markets (e.g. commodity DRAMs), to exploit opportunities in growing and higher margin markets (e.g. NAND flash, RDRAM, UHS SRAMs). Oh, yes, they are leaders in large screen flat panels and have a very strong position in full-featured cell phones.

Revenue	Intel MPG		Revenue	Samsung Tr KRW	M$
Architecture	7025		Semiconductor	4.12	3552
Communications	1066		Memory	3.16	2724
Other	1		Displays	2.37	2043
Total	8091		Telecom (Handsets)	4.61	3974
			Other	2.97	2560
			Total	14.41	12422

Operating Income		Margin Pct	Operating Income			Margin Pct
Architecture	3015	42.9%	Semiconductor	1.78	1534	43.2%
Communications	219	20.6%	Displays	0.84	724	35.4%
Other	-320	-32000.0%	Telecom	1.28	1086	28.0%
Total	2478	30.6%	Other	0.20	172	6.7%
			Total	4.06	3517	28.3%
Net Profit	1730	21.4%	Net Profit	3.14	2707	21.8%

INTERVIEW

The World's 2nd Largest Foundry: Providing SoC Solutions, DMR Interviews UMC's Vice President, Technical Staff, Tai Sheng Feng



United Microelectronics Corp. of Hsin Chu, Taiwan is a leading global semiconductor foundry that manufactures advanced process ICs for applications spanning every major sector of the semiconductor industry. UMC delivers cutting-edge foundry technologies that enable sophisticated system-on-chip (SoC) designs, including 90nm copper, 0.13um copper, embedded DRAM, and mixed signal/RFCMOS. UMC is a 300mm manufacturing leader with two advanced 300mm fabs in operation. Fab 12A in Tainan, Taiwan has been in volume production for customer products since 2002 and is currently manufacturing the industry's most advanced 0.13um and 90nm products. Fab 12A's production capacity is expected to reach 20,000 wafers by the end of 2004. UMC's second 300mm fab, UMCi, is located in Singapore's Pasir Ris Wafer Park. This second-generation 300mm facility is now in pilot production, and is expected to ramp to 10,000 wafers per month by year-end 2004. To get a better understanding of UMC, the *Denali Memory Report* interviewed Tai Sheng Feng, Vice President, Technical Staff at UMC.

Denali Memory Report: UMC has announced an aggressive wafer start expansion program. How will you boost capacity? More 300mm wafer starts?

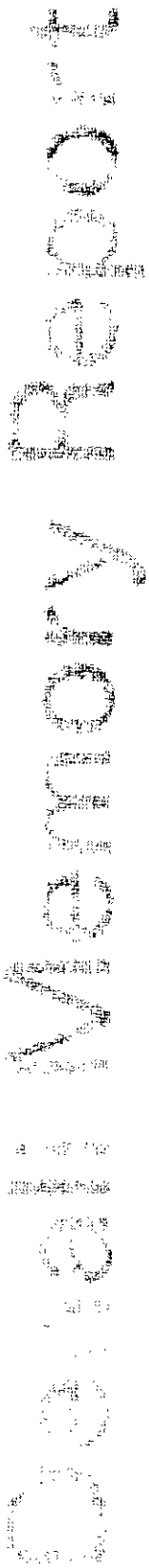
Tai Sheng Feng: There are two major components of the plan. UMC's Capex for 2004 is on the order of $2.1B. The majority of this investment—around 80 percent—will be invested in our 300mm fab. The remaining 20 percent will be invested in optimizing our existing 8-in fabs and for R&D.

DMR: You're convinced that 300mm is the most productive manufacturing strategy?

TSF: That's correct. If you look at the example of DRAMs—Powerchip, a major Taiwan DRAM company being a good model, three years ago they were not profitable. In the years since, they have shown dramatic improvement. A major reason for this change is that two years ago, they made major investments in 300mm manufacturing capacity and realized the resulting reduction in their cost structure. The same is true of Intel, which in 2000 and 2001 made major investments in 300mm capacity, despite the economic downturn.

UMC also has made major investments in 300mm beginning in 1999 with a 300mm partnership with Hitachi. We decided that for future business growth this was a prudent path. In addition, we recently acquired a seventh 8-in. fab from Silicon Integrated Systems Corp. in the Hsin Chu Science Based Industrial Park. Instead of building a new fab, which would take 12 to 18 months to complete, an immediate way we saw to increase capacity was to purchase an existing fab. With SIS we acquired a customer as well as additional manufacturing capacity.

DMR: It would appear from the SIS acquisition that Integrated Device Manufacturers (IDMs) would want UMC



to take over their manufacturing capacity and concentrate on design. Is this something you expect other IDMs to do?

TSF: That's something we've certainly done in the past. Four years ago, UMC merged five companies into a single corporation from UMC, USC, UTEK, USI, and UICC. In Japan UMC acquired the Nippon Steel DRAM fab and converted it into a profitable foundry operation. In the future if there is an opportunity that presents itself, we'll certainly consider it depending on our requirements. The SIS deal was favorable since UMC acquired a fully equipped fab through the issuance of 357 million new shares valued at approximately $515 million, compared to $1 billion or more to build a new fab.

DMR: Do you have a strategy for helping an IDM migrate from a fab to fab-lite to foundry?

TSF: No matter the business strategy of our customer—IDM, fab-lite, fabless—we work to fulfill their foundry requirements. We don't have a formal program for migrating customer from owning a fab to fab-lite, to fabless. This strategy is the sole responsibility of our customers who are best able to judge their manufacturing requirements. If a foundry provides the lowest cost, and best in class service, the IDM will make the decision based on whether their value add is in design or manufacturing and will choose accordingly. The best example of a successful outsourcing strategy is Hewlett-Packard. Today, they focus on marketing and outsource the bulk of their PC manufacturing to Taiwan. If you're driven by providing the most cost-effective manufacturing for your customer, you will get market share.

Capacity Expansion & Corporate Alliances

DMR: What is UMC's strategy toward building fab capacity outside of Taiwan?

TSF: UMC has expanded outside of Taiwan. Besides our fab in Japan (UMCJ), UMC has a 300-mm fab in Singapore, which by the end of the year will be producing 10k wafers per month. With our international sales and product support offices in the U.S. and Europe we have the ability to serve our worldwide customers. The fabs are mostly here in Taiwan, but the customer support, marketing and sales is spread broadly into all major markets.

DMR: Was the Singapore fab a UMC investment or a partnership with others?

TSF: The fab was a joint venture investment among the Singapore Government's Economic Development Board (EDB), Infineon, and UMC. Six months ago Infineon decided to withdraw from the investment to focus on DRAM. UMC guaranteed them production capacity and we acquired their share of the venture. EDB still owns a minor stake in UMCi, though UMC has 85 percent controlling interest.

DMR: In what alliances are you engaged for new process development such as your past involvement with IBM? What's the status of these alliances today and your plans for the future?

TSF: The UMC-Infineon-IBM alliance you referred to was a partnership to develop 0.13-micron process technology in 2000. Today, we're more focused on partnerships to enable successful right first time silicon SoC designs in the shortest time possible, not so much joint process development but time-to-market reduction methodology. This includes partnership with design companies, EDA tool vendors, and IP vendors. We also consider our customers as partners. We grow with our customers.

DMR: The capacity in the industry is tightest at the lower geometries: 0.13 and smaller. Will your investment strategy target these smaller geometries exclusively? Or will there be continued investment in larger geometries as well?

TSF: Most of our new investment will be for advanced process technology at the smaller

geometries. There is a simple reason for this. Our goal is to provide a total solution for SoC designs. In these designs, you will see increasing numbers of circuits being integrated into a single chip. To make this cost effective, advanced technology is absolutely required.

The Future is System on Chip Designs

DMR: Could you explain UMC's SoC program?

TSF: To build a successful SoC component, three core competencies are required. You have to have manufacturing excellence—high yield, low cost per die, etc. Secondly, you have to offer the latest advanced process technology—for example copper interconnect. The third element that is demanded is intellectual property (IP). We have aligned ourselves with the major IP providers to ensure all the fundamental building blocks these IP vendors supply are available and silicon proven in UMC processes.

DMR: What do you consider the critical IP building blocks UMC needs to offer their customers?

TSF: It depends on the market segment you're addressing. We license the ARM processor used in most wireless voice applications. We also license Rambus interconnect and memory technology. We are working with the top ten IP vendors to identify the key IP we need to provide in our advanced technology in the near future.

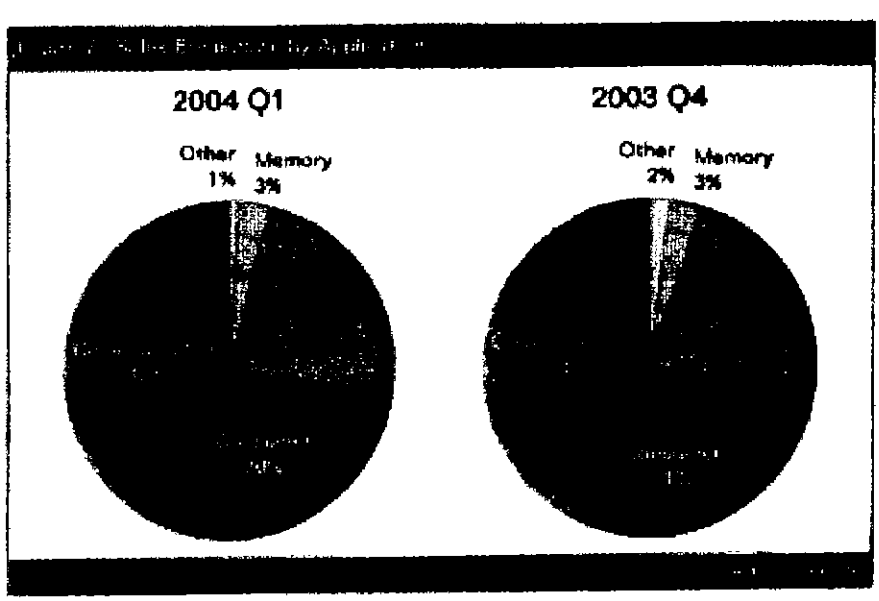
DMR: Does UMC develop any of its own IP?

TSF: We do develop our own process-sensitive IP. For example, we have developed e-fuse—electrical fuse memory—and A-to-D and D-to-A converters, all of which are sensitive to the semiconductor process. We also collaborate with partners to develop IP.

DMR: Have you developed your own SRAM, embedded DRAM, or embedded flash, or are these components you source from partners?

TSF: For embedded flash we work with a third party. For the 1T SRAM our partner is MoSys. However, we do build our own 6T SRAM memory.

DMR: You mentioned UMC developing advanced technology and cited copper as one example. What about other technology such as strained silicon, silicon-on-insulator (SOI), etc.?



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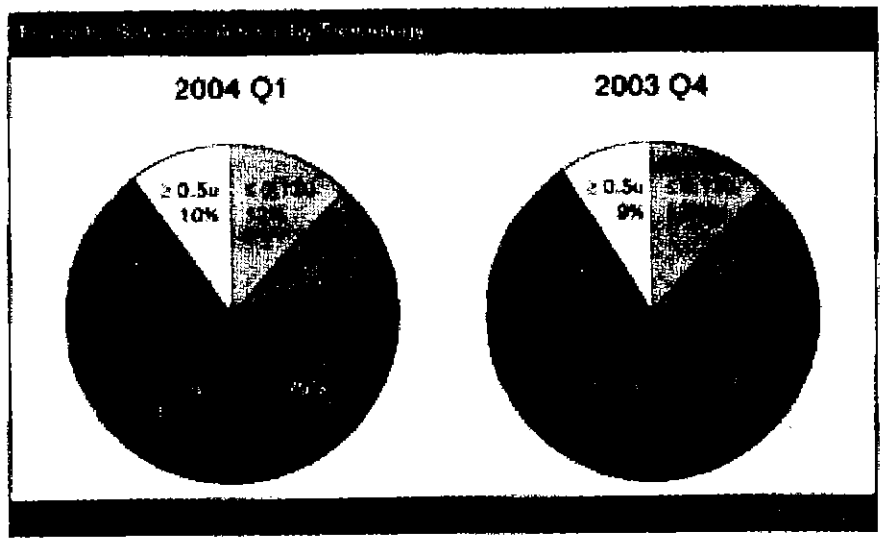

TSF: Strained silicon's purpose is to enhance performance of circuit elements. We have a team looking at strained silicon and ways it can be used to enhance circuit performance. However, ultimately we develop the process technology our customers are going to require for their future products. Whatever it is we will work with our partners and customers to develop.

Partnering for Success

DMR: The strategy among foundry suppliers is to cull their customer base to do more business with fewer customers as foundry capacity has grown tight. What is UMC's strategy in this regard?

TSF: Our strategy has always been to work with market leaders for each major market sector. By engaging with market leaders we are able to partner and grow with these customers over the long run. If a customer with a modest volume product wants to use the latest process technology, any foundry would have to carefully evaluate the long-term benefit the customer's design might afford before engaging.

DMR: Who are the market leaders you're engaging with currently? What market segments do they address consumer, communications, computing, etc?

TSF: The market segments demanding advanced technology include FPGAs, microprocessors, graphics controllers, and baseband circuits for cell phones. UMC is well aligned with the leaders in each of these segments.

DMR: These would include NVIDIA and Xilinx?

TSF: We have always been vocal about Xilinx being our close partner for their advanced technology products. For other segments, we are also working with customers of the same caliber.

DMR: What's the status of UMC's 90nm process? Are you in production? How long have you been in production? When will your 65nm process begin to see wafer starts?

TSF: Our 90nm process is fully qualified and we have several customers already in pilot production. Our first successful silicon for customer products on 90nm was with Xilinx in March of 2003. We're currently engaging with over five customers to run our 90nm process. We are running 90nm on our 8-in as well as 300mm lines. As for our 65nm process, pilot production is scheduled for the middle of 2005 according to our production roadmap.

DMR: What is driving the demand for 90nm? Is it because designs are huge and require the smaller process for a smaller die, or is it for performance reasons? What is the major consideration for customers wanting 90nm?

TSF: Customers are putting more features into their designs and for a larger design customers can maintain the same die size, thus providing a cost savings (per transistor) over building the same design in a larger process. Cost is the overriding factor and combining 90nm with 300mm wafers is a means of driving down the cost of a die.

A Unique China Strategy

DMR: TSMC is making investments in China. SMIC, who has become a major producer in China, is nearly as large as Chartered. China is not to be ignored. What has UMC said about their plans for China?

TSF: UMC has no current plans to expand into China. But, UMC has an alliance with He Jian Technology in the Suzhou region of China. They are producing at a rate of 20k 8-in. wafers a month. We refer our customers to them and they refer their customers to us. We are not in competition with them but have a mutually beneficial relationship. As you know, today fab utilization is 100 percent. Lacking additional capacity we refer our customers to our alliance partner in China. We coordinate our business development with He Jian.

DMR: Are there any other alliance partners you're using to offer additional capacity to your customers?

TSF: We're only working with He Jian currently. They have an aggressive expansion plan in place.

DMR: Commodity DRAM vendors have a limited product mix flowing through their fabs at any one time. A foundry has a much wider variety of product it has to accommodate. How many different types of products is it practical for a foundry to produce at any one time?

TSF: Normally, we only concern ourselves with process technology not the different types of products flowing through the fab. A 0.18-micron CMOS process at our fab might have between 20 to 30 customers building product on this process. They are all using the same process flow.

Fab	4Q03	1Q04	2Q04E	3Q04E	4Q04E
Fab 6B	88	88	88	86	86
Fab 6A/B	196	196	196	196	200
Fab 8C	90	90	96	98	105
Fab 8D	54	58	61	65	72
Fab 8E	98	98	101	102	102
Fab 8F	81	81	81	92	95
Fab 8S	0	0	0	50	75
Fab 12A	65	65	90	120	127
Subtotal	672	677	711	820	862
UMC	0	3	9	27	60
TOTAL	672	680	720	847	922

units in thousands (8" wafer eq.)

DMR: If a customer has a special process step requirement—high voltage or RF, how do you handle this requirement? Can you incorporate it into your flow?

TSF: Depending on the business potential for the special process step, we certainly will try to accommodate the request. You mentioned high voltage. We have worked with a design partner in the early stages to develop a high voltage process step addition. Today, there is strong demand for this capability. Three years ago when we made this investment, we were looking at the growing trend for flat panel displays to replace CRTs. These flat panel displays needed high voltage drivers, which we co-developed with our design partner. That market has become huge. When we see such high volume future demand we will work with our customers to accommodate process step additions.

Playing to Core Competencies

DMR: What are UMC's core competencies that attract customers? Is it fast time to market, low-defect density and high yield?

TSF: Our company's motto is "the foundry of choice." We like to think that when a customer chooses a foundry they think first of UMC. Why would customers make this choice? UMC has acquired knowledge in system design and architecture to provide a complete SoC solution to our customers. The process technology solution must be complemented by a silicon-proven design solution. To achieve this end we work with EDA vendors to get an effective design flow. We work with IP vendors to ensure their IP is optimized for the UMC process technology.

To explain it differently, you might consider why Taiwan-based companies can make the foundry business profitable. If you look at semiconductor companies in Korea and Japan, they build memories and consumer components but have never made a successful foundry business. Success in the foundry business not only requires process technology, it demands expertise in managing internally all the different customer parts being built at one time. Memories are simple, one common product being produced in very high volume. With a foundry there is a complex set of logistics controls that need to be in place to be successful. UMC has built this expertise over the past five years and we're good at what we do.

DMR: A 300mm wafer is very large and holds a large number of die. Do all your customers need this production capability or do you have methods of putting more than one design on the same wafer?

TDF: This capability of putting multiple designs on a single wafer is something done during shuttle runs to reduce costs, but it's typically one customer doing different designs. It's a method for verifying their design and reducing mask costs. For volume production, the customer will tape out a dedicated mask set. As far as who needs 300mm, the larger die-sized SoC designs will realize the greatest productivity gains, so we are migrating those designs first.

DMR: What about your strategy regarding structured ASICs.

TSF: Our fabless customers are not using structured ASIC. However, our partner Faraday is a fabless ASIC customer. The purpose of structured custom is to bridge between pure ASIC and FPGA to reduce the overall mask costs and time to market. We are working with Faraday to examine the potential business for UMC in this technology.

DMR: Where are the bulk of your leading edge technology design starts coming from?

TSF: For advanced process technology, our greatest demand is coming from customers in the U.S. for Graphics, FPGAs, etc. The leading companies are still in the U.S.

DMR: We would like to thank Mr. Feng for taking time to share his insights with us.

Denali

NOTICE

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Monday, June 7, 2004
San Diego Convention Center
3:00pm-9:00pm
DAC Rooms 31ABC, 32AB

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3:45pm	User Presentation	Sean Smith Cisco Systems, Inc.
	User Presentation	Anand Chavan Agere Systems, Inc.
	User Presentation	David Keates Intel Corporation
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6:45pm	User Presentation	Ramneek Real TAEC North America
	User Presentation	Srinivas Pattamatta Philips
[illegible]	[illegible]	[illegible]
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Don't forget to visit us at DAC:

Booth & Demo Suite #1945

And, who could forget the Denali DAC Party:

www.denali.com/dacparty.html

Tuesday June 8, 2004
Starting at 8:00 PM
On Broadway, located in the Gaslamp Quarter